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Susanne Jakob
Dipl.-Ing. Helge Drumm

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B. Vogler / M. Roßberg / R. Herzer

A fully integrated 600V SOI Half Bridge IGBT Gate Driver IC

POWER ENGINEERING

Abstract

The design, functionality and measurements of fully integrated 600V half bridge IGBT gate driver IC is presented. The two-channel High Voltage IC (HVIC) target different motor drive systems for low power and medium power applications. Dielectric device isolation and the detailed circuit design ensure operation up to a temperature of 200°C. Robust signal processing has been given highest attention at all design stages. A dedicated signal reconstruction topology is presented to provide maximum immunity against parasitic coupling from the power plane. The measurements confirming the safe operation of the IC.

Introduction

Intelligent Power Module (IPM) solutions for medium power applications (600V, <50A) are aimed at high volume markets, where system costs and geometric size per function are the most relevant parameters. IC-based designs are thus replacing conventional hybrid IGBT and MOS drivers [1] [2] [3] [4].
Due to the high production numbers, fully integrated solutions are feasible which combine both driving circuitry and power bridges on a single die [5]. Widely accepted gate drive ICs rely on conventional junction isolation to achieve 600V blocking voltage and to shield the high side from the offset voltage [6] [7]. Though the market has shown considerable interest in these HVICs, the junction isolation entails certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [8] [9] [10] but it cannot be resolved completely. Also, increasing pn leakage currents typically limit the operation temperature to 150°C.

600V SOI Technology

A high voltage SOI platform, on the other hand, can provide complete latch-up immunity since all active devices are dielectrically insulated. This enables the operational temperature range to be considerably extended. The chips were made with a 600V SOI foundry process [11] [12].
Fig.1 shows a schematic cross section of the 600V SOI technology. The regular CMOS- circuits of low side and high side based on quasi-bulk-transistors in fully isolated silicon islands. The active silicon is thick enough to prevent the punch-through from the backside space charge region to the front transistors.

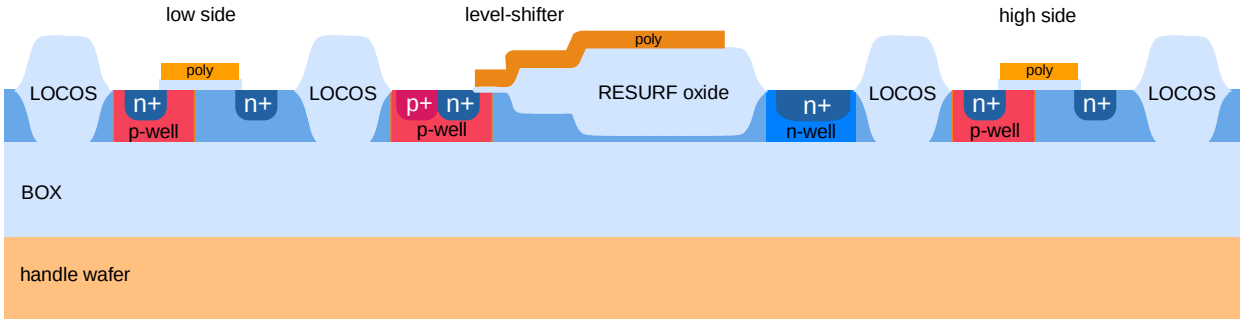

Fig.1 Schematic cross section of the foundry HV SOI technology [11] [12]

The keys to the high breakdown voltages are the thick buried oxide layer and the selective layer thinning in the drift region of the high voltage devices [13] [14]. Figs.2 and 3 illustrate the operation principle. While the lateral ionization paths are the same in both cases, the carrier multiplication due to vertical field components is drastically reduced in Fig.3 because of the reduced vertical avalanche path length.

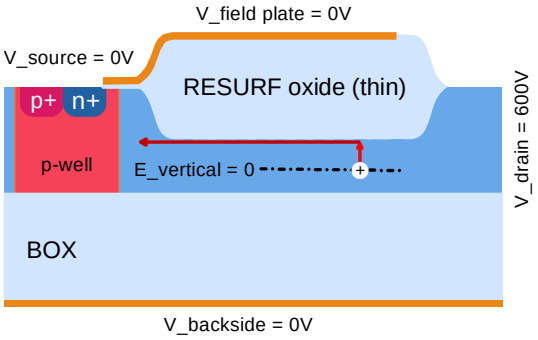

Fig.2 Vertical and lateral avalanche path in thick active silicon

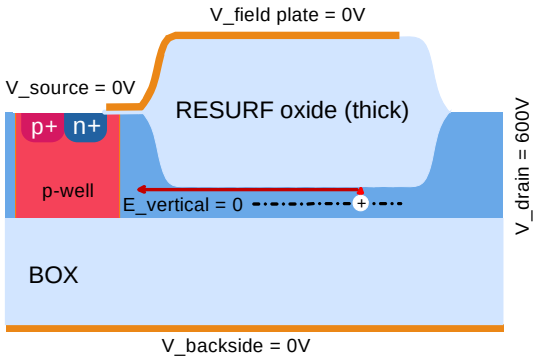

Fig.3 Vertical and lateral avalanche path in thin active silicon

System and HVIC design

Fig.4 shows a block diagram of the target two-channel power conversion system. The topological blocks to be integrated into a gate drive HVIC are marked. Depending on the different applications six-pack and seven-pack-driver ICs (e.g. for three-phase power conversion systems) are also possible, as well as additional blocks such as bootstrap-diodes, charge-pumps for power supply and V_{CE} detection diodes. The IC block diagram is given in Fig.5. Input interfaces (IIF) implement logic thresholds for direct connection to 5V or 3.3V micro controllers.
The IC contains an additional block for input signal processing (input mode logic), that enables to run the IC with both driving modes for input signals, either with two independent input signals for BOT- and TOP-channel [15] or to use only one input signal [7], which are common in today's gate driver ICs. If the second mode is activated the input logic generates the signal pattern for both TOP- and BOT-channel from the input signal applied at the _TOP/IN-Pin. The IC recognizes automatically which mode is desired, by monitoring the signal level at the _BOT-Pin.

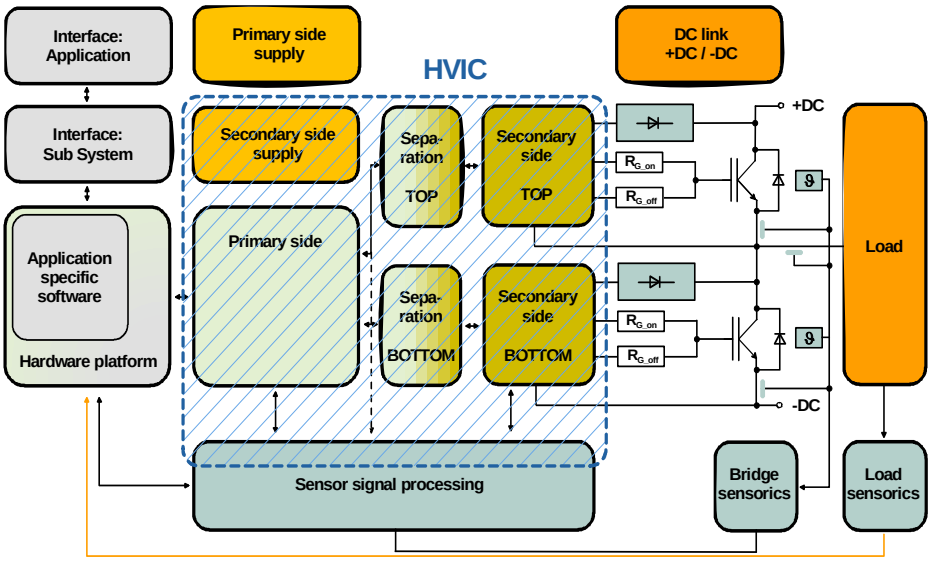

Fig.4: Power Conversion System showing gate driver HVIC integration area

If the voltage is lower than the monitoring threshold 10V, the input logic interprets the signal as a correct micro controller pattern for the BOT-channel. If the voltage is always above the threshold voltage the _BOT-Pin is deactivated and the driving signals for BOT- and TOP-channel are generated from the signal at the _TOP/IN-Pin. An internal pull-up resistor pulls the input to the supply voltage when the _BOT-Pin is not connected to the controller so there is no need to bond the Pin when it's not used.
An interlock time is usually implemented in the external drive controller pattern and there is also a hardware interlock in the gate driver. Both methods minimize cross-currents in the external power bridge. Logic and error management generate the appropriate internal signals. These take into account under voltage lockout (UVLO) as derived from a bandgap-stabilized reference, and external analog sensor signals such as shunt current or temperature monitoring. The branch delay times of the main channels TOP and BOT are delay-matched to ensure synchronized switching.

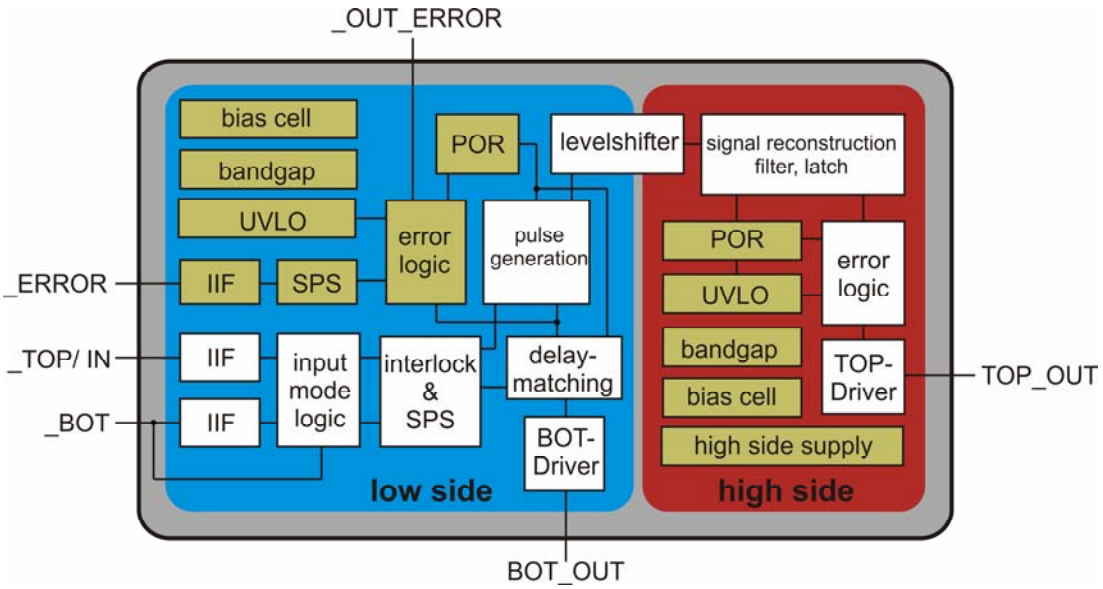

Fig.5: Block diagram of the half bridge gate driver IC

Level-shifter design and IC Layout

The single most important internal function of the gate drive IC is to transmit signals from the controlling low side to the high side. The signal reconstruction scheme at the high side, in particular, where the transmitted raw pulses are interpreted and converted into valid control patterns, is of fundamental importance. The reconstruction scheme has to separate signals from any voltage or current disturbances which couple back into the IC from the electromagnetically polluted system environment. The raw signal transmission uses two conventional cascode switch configurations as shown in Fig.6. The 600V HV transistor isolates the low side from the high side. As soon as the transistor M_1 opens a cross-current flows from the high side supply Vdd_hs to low side ground (gnd_ls). The current is limited in M_1 by source feedback over R_{lim}. The voltage drop across R_hs is the high side raw signal (V_{OUT}).

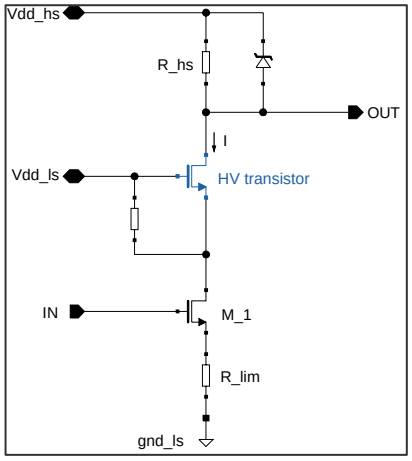

Fig.6: Level-shifter cell (twice per channel for differential transmission)

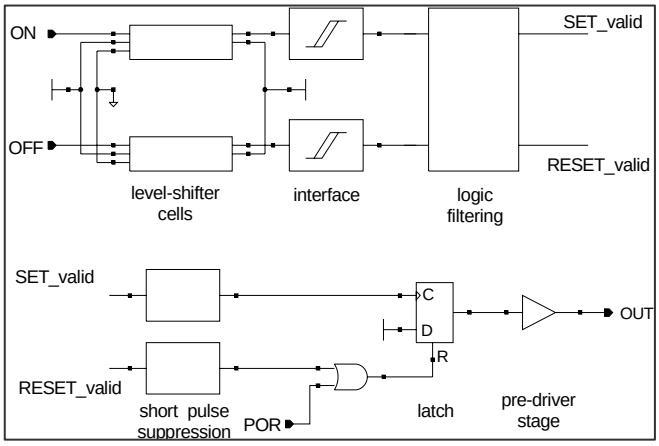

Fig.7: Signal reconstruction topology

A differential scheme is necessary because of common mode currents flowing through the cell during every dv/dt event between low side and high side. These events are caused by normal switching on or off of the respective channel or by parasitic coupling between channels. The signal reconstruction which has been developed and shown in Fig.7 relies on individual recognition and processing of the two raw signals rather than a conventional conversion, from differential to single-ended, using latching stages. The high robustness obtained for the level-shifter is due to the combination of three factors: wide signal swings with interface hysteresis; simple, yet effective logic filtering of common mode signals; and short pulse suppression. This result has been proven by experimental results presented later on. The signal POR (power on reset) in Fig.7 ensures defined power-up of the latch that is storing the drive information.

Fig. 8 shows the layout design of the half bridge gate driver IC. The 15 level CMOS-SOI process includes two metallization levels. An additional high voltage module provides special devices such as HV-transistors for level-shifter applications and HV-diodes for high side power supply (bootstrap diode, Fig.8) or sensing applications (V_{CE}-monitoring e.g.). The described level-shifter and signal reconstruction scheme is marked in Fig.8.

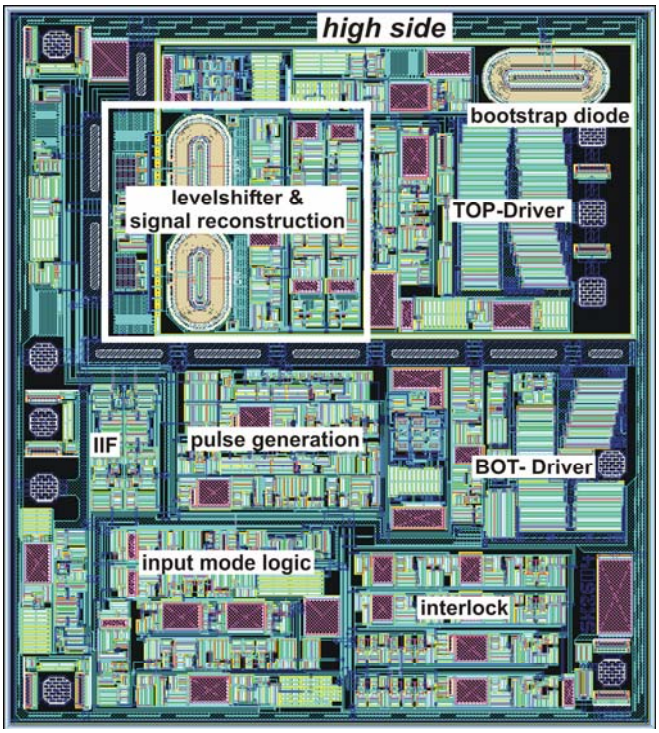

Fig.8: Layout of the half bridge gate driver IC (chip size approximately 4mm^2)

Measurements

All high voltage measurements were taken with the gate drive ICs operating on a 600V, 10A half bridge module with CAL free-wheeling diode. The module output is connected to an individual resistive-inductive load. Fig.9 shows a photograph of the measurement setup.

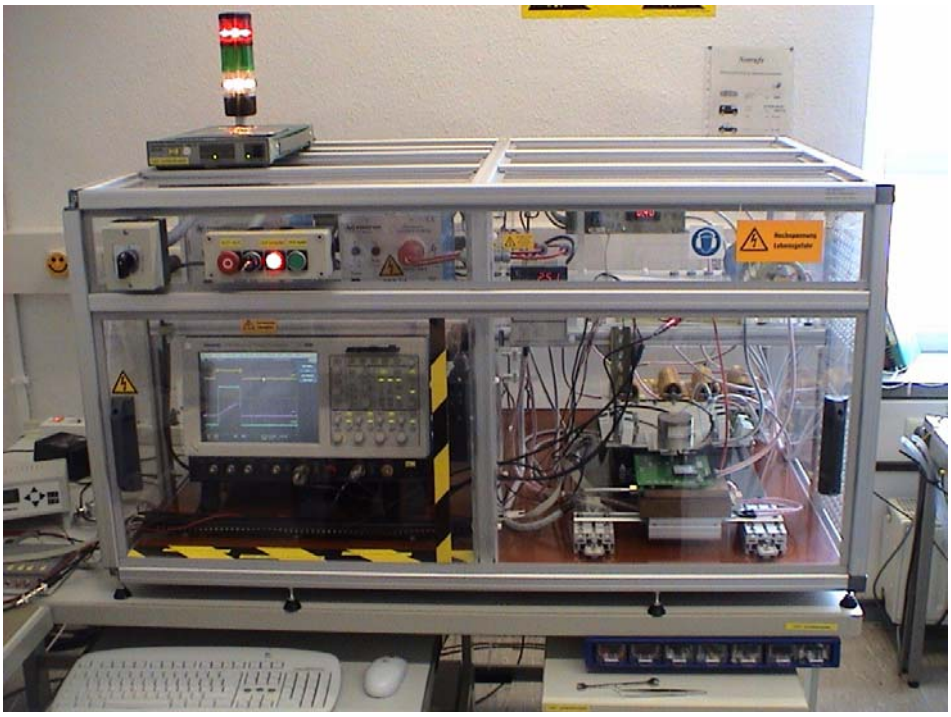

Fig.9: High voltage measurement setup

The switching of BOT- and TOP-channel at active interlock is demonstrated in Fig10. The TOP switch turns on (OUT_{TOP}) at a valid on-signal (IN_{TOP}) and turns off if an on-signal occurs at IN_{BOT} to avoid a short circuit in the half-bridge (defined safety regime).

Several potentially hazardous situations that exceed the limits of regular operation have been tested. Fig.11 shows as a worst case scenario an intended, increased coupling of magnetic fields of the load inductivity on the input signal of 3.3V. Additional the load current oscillations were amplified by the stray inductivities of the measuring setup. Although the noise amplitude is twice as much as the input signal the chip internal filtering and signal reconstruction interprets the noise as invalid signals.

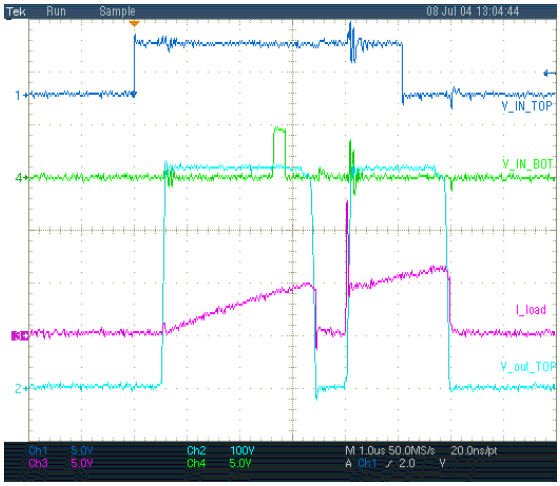

Fig.10: Interlock mode operation at V_{DC+}=400V (BOT/TOP)

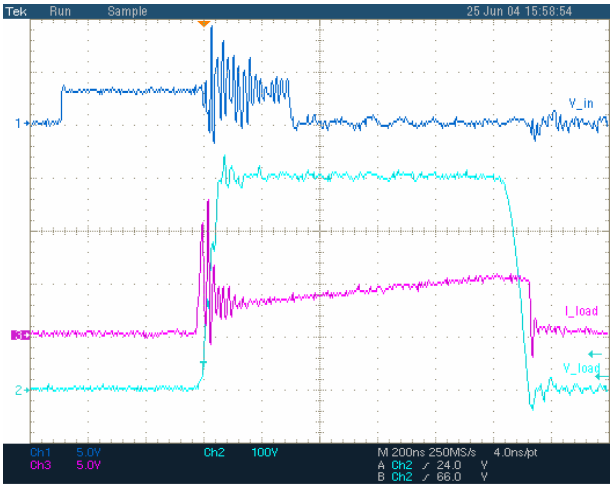

Fig.11: Double Pulse measurement with Increased noise coupling on 3.3V input signal

Another measurement is shown in Fig. 12 of the IGBT turning on into a hard short circuit and generating harsh current and voltage transients. Internal shunt monitoring produces a reaction as soon as the current rises above the short circuit threshold. A local error signal I_ERR tracks the fault. The global error signal ERR_OUT is generated and sent back to the micro-controller and the IGBTs are turned off.

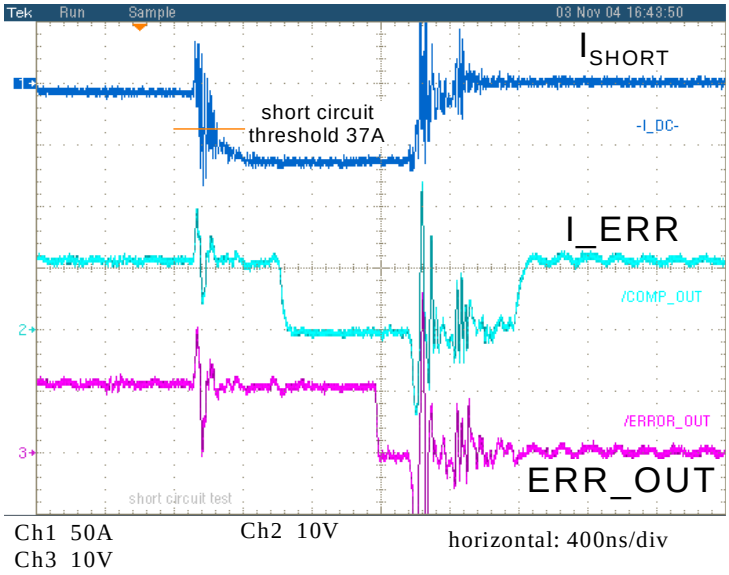

Fig.12: Short circuit management (hard short circuit)

Conclusion

High voltage SOI technologies are available that allow monolithic integration of gate drive HVIC for 600V systems. Specific work on signal integrity and robustness against coupling from the power environment has led to safe HVIC operation under all conditions tested: low voltage input, high output dv/dt, short circuit and driver stage temperatures higher than 200°C.

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Authors:

Dipl.-Ing. Bastian Vogler *
Dipl.-Ing. Matthias Roßberg**
PD Dr.-Ing. habil. Reinhard Herzer**
*TU Ilmenau, Germany; P.O. Box 10 05 65, D-98684 Ilmenau
**SEMIKRON Elektronik, Germany; Sigmundstrasse 200, D-90431 Nürnberg
Phone: +49-3677-69-3224
FAX: +49-3677-69-3777
E-mail: bastian.vogler@tu-ilmenau.de